Simultaneous neural signal recording from many neurons has a wide range of applications ranging from the study of complex biological neural networks to brain controlled neural prostheses to treat spinal cord injuries by restoring limb movement [1]. Wireless transmission of the recorded signals combined with on-chip neural spike sorting (a.k.a. spike sorting) and versatile wireless telemetry (raw and compressed data) has not been reported yet. This paper presents one such system with the capability to record, process and wirelessly transmit multiple neural signals real-time.

The chip is composed of eight 16-channel front-end blocks, data serializing circuits, a DSP for on-chip spike sorting, digital MUX, a second amplifier and a SAR-ADC (Fig. 7.6.2). The amplifiers recorded and transmitted without any additional processing. The chip operates in one of the two modes. In sorting mode, a selected channel is connected to the on-the-fly spike sorting block and the extracted features of the spikes are transmitted for off-chip classification. In streaming mode, all the sampled data from the 128 channels are recorded and transmitted without any additional processing.

The front-end block consists of preamplifiers, buffers, an analog MUX, a second amplifier and a SAR-ADC (Fig. 7.6.2). The amplifiers are designed to have variable gain and bandwidth to meet the requirement of biological experiments. 16-to-1 multiplexing is chosen to minimize the power-area product of the entire system [6]. The preamplifier use cas-coupling to reject the large dc offset occurring at the electrode-tissue interface [4]. The gain of the preamplifier is 40dB, and the second amplifier following the analog multiplexer provides an additional gain of 17dB to 20dB according to external con-40dB, and the second amplifier following the analog multiplexer pro-

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Figure 7.6.1: Block diagram of the integrated neural recording system.

Figure 7.6.2: Schematic of 16-channel front-end blocks (Sequential turn-on scheme is used to reduce the power consumption).

Figure 7.6.3: Proposed spike sorting algorithm.

Figure 7.6.4: Block diagram of an on-line spike sorting engine.

Figure 7.6.5: Block diagram of UWB transmitter and receiver.

Figure 7.6.6: Chip micrograph and performance summary.

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Figure 7.6.7: Measurement results of the IC with neural signal from a snail brain.