Predictive Control Formulation for Achieving a Reduced Finite Control Set in Flying Capacitor Converters

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Abstract-Multilevel Converters (MCs) have emerged as a promising alternative to traditional two level converters. These topologies present a better output voltage quality due to the reduction of the voltage steps by increasing the voltage number levels. Within the MC family, flying capacitor converters present a special attraction due to the easy way to increase output voltage levels by adding cells. Recently model predictive control algorithms have reached a special interest in MCs applications. In particular, finite control set predictive control algorithms applied to flying capacitor converters have shown that it is possible to achieve a good performance in the control of capacitor voltages and output current. For that purpose, at each sample time the controller explores all the switching states and determines the optimal one to be applied. However, the number of switching states grow exponentially in relation to the number of cells. This increases the time that the algorithm takes to find the optimal switching state. In this paper we present an offline strategy to reduce the number of switching states to be explored in a finite control set predictive algorithm by using only those which produce that the system state point towards to the reference. Moreover, a sampling period design is presented to guarantee that the system state remains inside of a positive invariant set.

I. INTRODUCTION

Multilevel converters (MCs) have emerged as an important technology in many industrial applications. The main reason for this is that MCs are able to operate at far higher power levels and also provide output voltage and currents with lower distortion than their two level counterparts [1].

In particular, flying capacitor converters (FCCs) have attracted significant attention [2] because of its special feature such as to have a unique dc-link voltage, easy way to increase the output voltage levels by adding cells and when an internal fault occurs, currents decay quickly, since the associated capacitors seek voltage balance [3]. However, a balancing of the capacitor voltages is required in FCCs to achieve a uniform distribution of the transistor blocking voltage [4].

Recently, predictive control strategies [5] have been applied to power converters and multilevel converters in particular, see e.g. [6]–[10]. Advantages of using predictive control, when compared to traditional PWM methods, derive from the fact that changing operating conditions are explicitly accounted for. In [8], a model predictive control (MPC) strategy for FCCs is presented. The goal of this work is to control not only the output current but also the capacitor voltages and the current spectrum. For that propose, a cost

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function which takes into account the system state error is define. Moreover, a notch filter is applied to the error of the current in order to obtain a control of its spectrum. Finally, the controller minimizes this cost function by exploring a finite control set of switches to determine the optimal action to be applied. The elements of this control set depend on an exponential way of the number of cells. Thus, if the number of cells grows the controller will take a long time to find the optimal switching action to be applied. This hinders its use in many practical applications.

In [11], a hybrid model of a boost converter is presented. Here, the power system the converter is analyzed taking into account its nature, which presents discrete inputs (switching action) and continuous outputs (currents and voltages). In addition, a safe spherical boundary space around the reference point is presented. To guarantee the stability of the system by keeping the system state inside of this set, the maximum allowed radius of this sphere is subject to, for all system states inside of this region exist a discrete input which generates that the system state points inwards to the reference point.

This paper presents a constraint finite control state MPC algorithm, which presents a reduction in the switching states to be explored. This reduction is based on the analysis of the continuous model of the converter choosing those switching states which yield that the system state points towards to the desired operating point. This analysis is carried out off-line, so it does not imply an extra effort in the implementation for the controller. Furthermore, a sampling period design is presented in order to define an admissible error in the system. Finally, this analysis allows one to establish an invariant set when the reference is constant, that means when the FCC is used as a dc-dc converter.

The remainder of this paper is organized as follows: In Section II we develop the continuous and discrete model for a generalized *n*-cell FCC considered for the proposed strategy. Section III gives a brief of MPC algorithm applied to an FCC. In Section IV we present our proposed constraint finite control set Predictive Control strategy. Section V presents a specific design study and Section VI draws conclusions.

II. FLYING CAPACITOR CONVERTER

In this section we describe the flying capacitor topology in more detail and develop a model for the system.

Figure 1 shows a topology of a generalized single phase n-cell flying capacitor converter. Here it is possible to see how the cells are interconnected in a cascade way. As it was

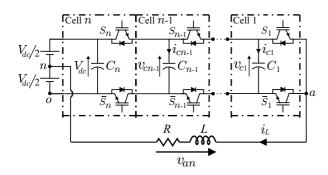


Fig. 1. Generalized n-cell FCC.

mentioned above, each cell i consists of a capacitor C_i and two switching elements S_i and \bar{S}_i which, at the same instant, cannot present the same state in order to avoid a short-circuit or an open-circuit in the cell.

The system is supplied by a dc-link voltage V_{dc} . It is important to note that the load is connected between the output point a and the middle point of the dc-link o. It is necessary to generate an alternating output current. It is important to note that if we consider only one cell, the FCC is turned into a traditional 2-level converter.

In a FCC it is necessary to control not only the output current i_L but also internal capacitor voltages. As the capacitor voltage in cell number n is imposed by the dc-link voltage $v_{cn} = V_{dc}$, we need to focus on the remaining n-1 capacitor voltages. Hence, for an n-cell FCC one can define a state variable model with n variables (the output current i_L and the n-1 capacitor voltages).

A. Continuous Time Model

As the two switches in the same cell work in complementary way, the state of this pair of switches can be represented only by the state of one of them. It can be expressed as follow:

$$S_i(t) = \begin{cases} 0 & \text{if } S_i = 0 \text{ and } \bar{S}_i = 1, \\ 1 & \text{if } S_i = 1 \text{ and } \bar{S}_i = 0. \end{cases}$$
 (1)

for all $i \in \{1, ..., n\}$.

Converter output voltage $v_{an}(t)$ is composed of different capacitor voltages v_{ci} combinations which depend on the switching state applied. Hence, the output voltage can be represented by:

$$v_{an}(t) = v_{c1}(t)S_1(t) + \sum_{i=2}^{n} (v_{ci}(t) - v_{ci-1}(t))S_i(t) - V_{dc}/2.$$
(2)

A similar situation is presented in the capacitor currents which are defined by:

$$i_{ci}(t) = i_L(t)(-S_i(t) + S_{i+1}(t)).$$
 (3)

Finally, a simple dynamic model of the system can be developed based on elementary circuit analysis of the electrical

topology shown in Fig. 1.

$$\frac{dv_{ci}(t)}{dt} = \frac{i_L(t)}{C_i} (-S_i(t) + S_{i+1}(t)), \tag{4}$$

$$\frac{di_L(t)}{dt} = -\frac{R}{L}i_L(t) + \frac{1}{L}v_{an}(t). \tag{5}$$

These equations can be rewritten as:

$$\frac{dx(t)}{dt} = Ax(t) + B(x(t))(t)u(t) + E.$$
 (6)

where

$$x(t) \triangleq \begin{bmatrix} v_{c1}(t) & \cdots & v_{cn-1}(t) & i_L(t) \end{bmatrix}^T,$$

$$u(t) \triangleq \begin{bmatrix} S_1(t) & \cdots & S_n(t) \end{bmatrix}^T,$$

$$A \triangleq \begin{bmatrix} 0 & 0 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & 0 \\ 0 & 0 & \cdots & -R/L \end{bmatrix},$$

$$B(x(t))(t) \triangleq \begin{bmatrix} \frac{-i_L(t)}{C_1} & \cdots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \cdots & \frac{i_L(t)}{C_{n-1}} \\ \frac{v_{c1}(t)}{L} & \cdots & \frac{(V_{dc} - v_{cn-1}(t))}{L} \end{bmatrix},$$

$$E \triangleq \begin{bmatrix} 0 & \cdots & 0 & -V_{dc}/2 \end{bmatrix}^T.$$

B. Discrete Time Model

To obtain a discrete time model of a FCC, we first apply forward Euler approximation to the capacitor voltage equation (4). This method assumes that the capacitor current $i_{ci}(t)$ is constant in a sample period h (see Fig. 2-a)).

$$v_{ci}[k+1] = v_{ci}[k] + \frac{h}{C_i} \left(-S_i[k] + S_{i+1}[k] \right) i_L[k]. \tag{8}$$

The continuous output current model can be transformed into discrete time using zero order hold approximation. In this case we are assuming that the converter applies a constant load voltage $v_{an}(t)$ in a sample period h (see Fig. 2-b)).

$$i_L[k+1] = K_a i_L[k] + K_b v_{an}[k].$$
 (9)

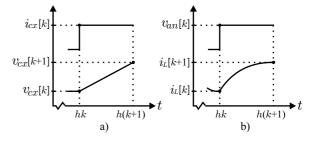


Fig. 2. Assumptions on the discretization of the model. a) constant capacitor current within a sampled period h; b) constant load voltage within a sample period h.

where the constant K_a and K_b are given by:

$$K_a = e^{-h\frac{R}{L}},\tag{10}$$

$$K_b = (1 - K_a)/R.$$
 (11)

and the output voltage $v_{an}[k]$ is defined by:

$$v_{an}[k] = v_{c1}[k]S_1[k] + \sum_{i=2}^{n} (v_{ci}[k] - v_{ci-1}[k])S_i[k] - V_{dc}/2.$$
(12)

Finally, the discrete time model for an n-cell FCC can be expressed via:

$$x[k+1] = Fx[k] + G(x)[k]u(t) + H.$$
 (13)

where

$$F \triangleq \begin{bmatrix} 0 & 0 & \cdots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \cdots & 1 & 0 \\ 0 & 0 & \cdots & 0 & K_a \end{bmatrix}, \qquad (14)$$

$$G(x)[k] \triangleq \begin{bmatrix} -h \cdot i_L[k] & \cdots & 0 \\ \hline C_1 & & & \\ 0 & \cdots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \cdots & \frac{h \cdot i_L[k]}{C_{n-1}} \\ K_b v_{c1}[k] & \cdots & K_b (V_{dc} - v_{C_{n-1}}[k]) \end{bmatrix},$$

$$H \triangleq \begin{bmatrix} 0 & \cdots & 0 & -K_b \cdot V_{dc}/2 \end{bmatrix}^T.$$

III. EXISTING MPC STRATEGIES

In this section, we present the standard way to apply finite control set MPC for FCCs (for further detail, see [12]).

The predictive control strategy is implemented in discrete time with sampling frequency $f_s=h^{-1}$. Firstly, for each sample time k we define the error vector via:

$$e[k] \triangleq \begin{bmatrix} v_{c1}[k] - v_{c1}^*[k] \\ \vdots \\ v_{cn-1}[k] - v_{cn-1}^*[k] \\ i_L[k] - i_L^*[k] \end{bmatrix}$$
 (15)

where $i_L^*[k]$ is the desired output current and $v_{ci}^*[k]$ are the, so-called "balanced" capacitor voltage references where its desired value is expressed via:

$$v_{ci}^*[k] = \frac{i}{n} V_{dc},$$
 (16)

where i refers to the cell number.

This capacitor voltage relationship is necessary to distribute uniformly the blocking voltage for each transistor [4]¹.

¹Recently, we have also investigated the use of MPC to drive FCCs to out-of-balance states [13].

 $\label{eq:table interpolation} \mbox{TABLE I}$ Switching states for a FCC of 1 and 2 cells

G 11 17 1		
Cell Number	Sw. States	Sw. Combinations
	μ	$u = [S_1]$
n = 1	$\mu = 0$	u = [0]
	$\mu = 1$	u = [1]
n = 2	μ	$u = [S_1 \ S_2]$
	$\mu = 0$	$u = [0 \ 0]$
	$\mu = 1$	$u = [1 \ 0]$
	$\mu = 2$	$u = [0 \ 1]$
	$\mu = 3$	$u = [1 \ 1]$

At each instant k, a measurement of the system state x[k] is used for the minimization of the following cost function:

$$J[\vec{u}[k], x[k]] = \sum_{l=k+1}^{k+N} e[l]^T Pe[l].$$
 (17)

where

$$P = diag\{\lambda, \cdots, \lambda, 1\}. \tag{18}$$

Here, λ is a design parameter, which allows one to trade current tracking errors versus capacitor voltage tracking errors. The decision variables are

$$\vec{u}[k] \triangleq \{u[k+1], \cdots, u[k+N]\}. \tag{19}$$

The vector $\vec{u}[k]$, thus, contains tentative switching actions over a horizon of finite length N.

The optimal switching action to be applied at time k+1, namely $u_{opt}[k]$ is obtained by minimizing $J[\vec{u}[k],x[k]]$. Then, at the next sample time, k+1, the cost function $J[\vec{u}[k+1],x[k+1]]$ is minimized using fresh state measurements. This gives $u_{opt}[k+1]$, etc.

IV. MPC WITH SWITCHING STATE REDUCTION

As shown above, in finite state set MPC the controller needs to explore the different switching combination of the vector $\vec{u}[k]$ in order to find the one which minimizes the cost function $J[\vec{u}[k+1],x[k+1]]$. For a general system of n cells and a prediction horizon of N, the amount of switching combinations, say SC, is:

$$SC = 2^{nN} (20)$$

Clearly, as the cell number n is increased, MPC algorithm will take a long time to find the optimal switch combination $u_{opt}[k]$. This hinders its use in many practical applications. To overcome this problem, we will next present an off-line strategy where only a reduced number of switching states to be explored. Our strategy (in certain cases) also guarantees that the system state will remain within a bounded region.

A. Basic Principle

Our proposal uses a sampled-data model, i.e., switching is only allowed at discrete instant k, and system variables are described in continuous time. We first define the switching

state μ which represents the n switching states. Table I shows it for n=1 and n=2.

Thus, the dynamic model (6) can be rewritten as:

$$\frac{dx(t)}{dt}^{(\mu)} = f^{(\mu)}(x(t)) = Ax(t) + B(x)(t)u(t) + E. \quad (21)$$

We bound the system state. For that purpose we introduce a set of n positive scalars $\{\delta_i\}$ and define a target region \mathcal{D} via:

$$\mathcal{D} = \{ x \in \mathbb{R}^n : |x_i - x_i^*| \le \delta_i \ \forall i \}, \tag{22}$$

where x_i refers to the *i*-th element of x.

To reduce the number of switching states to be explored by the MPC algorithm, we only use those combinations which point towards the reference $x^*[k]$ is necessary that the system satisfy the following condition:

$$\forall x \in \mathcal{D}, \ \exists \ \mu \ s.t. \ (x_i - x_i^*) f_i^{(\mu)}(x(t)) \le 0 \ \forall i.$$
 (23)

where $f_i^{(\mu)}$ refers to the *i*-th element of $f^{(\mu)}$.

We will newt show below that this FCCs with 1 and 2 condition is satisfied.

B. Sampling Period Design

To be certain that the state variables x(t) remains inside of the region \mathcal{D} , it is necessary to select the sample period h carefully. Considering the discrete time model presented in (13) one can determine the worst change that the system state can present. The worst case occurs when $x[k] = x^*[k]$. Thus, the the sample period h needs to be chosen such that:

$$\delta_i \ge \max\{|x_i^{(\mu)}[k+1] - x_i^*[k]|\}, \ \forall \mu, i.$$
 (24)

Otherwise, one can use (24) in order to determine the maximum error $\{\delta_i\}$ that the system will present for a given sample period h.

C. Example for a 1-cell FCC (2-level Inverter)

In a 1-cell FCC, it is necessary to control only the output current $i_L(t)$. For this, the controller can make use of SC=2 switching combinations. Now, it is necessary to accomplish the constraints presented above.

Firstly, for the switching state $\mu = 0$ we have:

$$-(x-x^*)\left(x+\frac{V_{dc}}{2R}\right) \le 0.$$
 (25)

Independent of the number of cell, output current can take only the following values: $i_L \in \{-\frac{V_{dc}}{2R}, \frac{V_{dc}}{2R}\}$. Thus, it is true that $(x+\frac{V_{dc}}{2R}) \geq 0$. Therefore constraint (22) is satisfied when $x \geq x_2*$.

Next, we can apply the same analysis for the switching state $\mu=1$:

$$-(x-x^*)\left(x-\frac{V_{dc}}{2R}\right) \le 0.$$
 (26)

Here, constraint (22) is satisfied when $x \le x_2*$. As a result of this analysis, for a 1-cell FCC, one can apply a switching state depending on the present output current stated $i_L[k]$ as it is showed in Fig. 3. Finally, if the sample period h and the error $\{\delta_i\}$ are adjusted as it is expressed in (24) and the

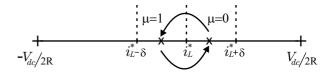


Fig. 3. Region \mathcal{D} and switching states distribution for a 1-cell.

switching states are applied as is shown in Fig. 3, one can guarantee that for a 1-cell FCC, $x(t) \in \mathcal{D}$ for all t > 0,i.e., \mathcal{D} is a positive invariant set [14].

V. APPLICATION TO A 2-CELL FCC

A. Analysis

Unlike the previous case, for a 2-cell FCC, it is necessary to control not only the output current but also the capacitor voltage of the cell number 1. For that purpose, this topology presents SC=4 switching combinations that can be applied. A similar analysis to that presented in the previous example can be applied in order to define when each switching state can be applied.

For $\mu = 0$, the following constraint must be satisfied:

$$\begin{bmatrix} 0 \\ -(x_2 - x_2^*) \left(x_2 + \frac{V_{dc}}{2R}\right) \end{bmatrix} \le \begin{bmatrix} 0 \\ 0 \end{bmatrix}. \tag{27}$$

This constraint is similar to the one presented in (25), To satisfy the restriction (27), $x_2 \ge x_2*$. Thus independent of $v_{c1}(t)$, the switching state $\mu = 0$ can be applied whenever the output current $i_L(t)$ is higher than its reference $i_L^*(t)$.

A similar analysis can be carried out to the remaining switching states (details are omitted for sake of brevity). Fig. 4 presents the allowable switching states μ as a function of the present state of the system. Here is possible to see that there are two regions $L^{(+)}$ and $L^{(-)}$ according to the direction of the current. Moreover, each region is divided into four quadrants which include the switching states μ that the controller can apply.

On the other hand, when we focus on the sample period h and its constraint presented in (24), the highest change outward from the desired equilibrium point is generated by the switching states $\mu=0$ and $\mu=3$. This means, that the worst condition is achieved when the 2-cell FCC works as a 2-level inverter. Thus, when the four switching states are taken into account by the proposed controller conform to Fig. 4, the system error will be lower than the generated by a 2-level inverter.

Finally, when the sample period h and the admissible error $\{\delta_i\}$ satisfy (24) and the switching states are applied conform to Fig. 4, for a 2-cell FCC, it can be guaranteed that $x(t) \in \mathcal{D}$ for all t > 0, i.e., \mathcal{D} is a positive invariant set [14].

As a result of this analysis, for a n-cell FCC one can be sure that switching states $\mu=0$ and $\mu=n-1$ satisfy the constraint (27). Then, the difference is presented in the division of the region $\mathcal D$ and how to distribute the switching states. Thus, the controller first has to discern, for each k instant, in which part of the region $\mathcal D$ the system is positioned. Then the MPC strategy is applied by exploring only

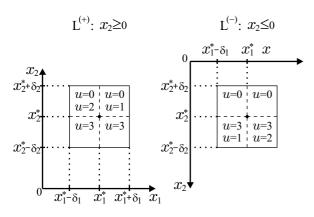


Fig. 4. Region \mathcal{D} and switching states distribution for a 2-cell.

the available switching states μ . Finally, the cost function J[k] presented in (17) is minimized to determine the optimal switching action, $u_{opt}[k]$, to be applied.

B. Simulation Study

To verify the performance of the proposed strategy, simulation studies were carried out on a 2-cell FCC. The electrical parameters used are: $C_{yj}=220[uF],\ R=10[\Omega]$ and L=1[mH] and a dc-link voltage of $V_{dc}=400[V]$. According to (16) the capacitor reference is $v_c^*=200[V]$. A constant current reference $i_y^*=5[A]$ is considered. Thus, the desired operating point is $x^*=[200\ 5]^T$.

The proposed strategy is applied using a sample frequency of $f_s = 20[kHz]$. Hence, to satisfy (24) the region \mathcal{D} is limited by $\delta = [0.62 \ 1.2]^T$. Furthermore, the proposed MPC algorithm is adjusted using a weight factor $\lambda = 0.01$ and N = 1. The initial conditions is $x(0) = [200.5 \ 5]^T$.

Fig. 5 depicts the operation of the 2-cell FCC controlled by the proposed MPC algorithm. Initially, the system is operated as a 2-level inverter, that is the controller only is using the switching states $\mu=0$ and $\mu=3$. Despite this situation, the system state remains inside of the region $\mathcal D$ as is shown in Fig. 5-b). Capacitor voltage $v_c(t)$ stays constant and the output current present the highest allowed change. This behavior is the same presented in Fig. 3.

Afterwards, in the instant t=1[ms] the controller starts using all the switching states conform to Fig. 4. Under this situation, the error of the output current $i_L(t)$ is decreased and the capacitor voltage $v_c(t)$ starts varying around its operating point. Moreover, one can see, for both conditions, how the system state remains inside of the region \mathcal{D} .

In Fig. 6 the prosed MPC method compared to standard MPC algorithm is shown. At the beginning, the optima switching action, $u_{opt}[k]$, to be applied is determine by exploring all the switching states. Under this situation, the system state present the behavior depicts in Fig. 6-b). Then, at the instant t=1[ms] the switching states to be explored is reduced as is proposed by our method. Fig. 6-c) presents the system state behavior for this condition. In both case, the system state is remained inside the region $\mathcal D$ producing a similar switching state patron and also a similar tracking error. This proves that it is not necessary to explore all the

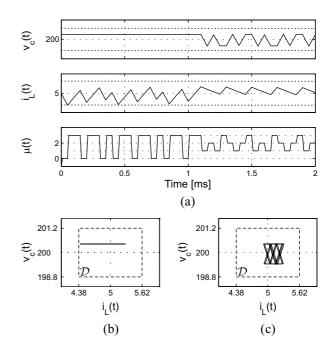


Fig. 5. Proposed MCP algorithm. (a) Capacitor voltage $v_c(t)$; output current $i_L(t)$; switching states $\mu(t)$. (b) System state controlled by considering only $\mu=0$ and $\mu=3$ (0< t<1[ms]). (c) System state controlled as it is proposed (t>1[ms]).

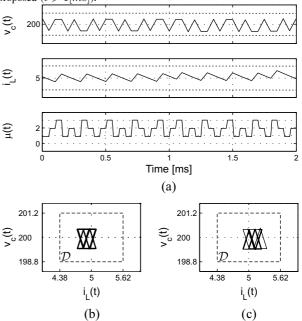


Fig. 6. Proposed MCP algorithm compared to standard MPC. (a) Capacitor voltage $v_c(t)$; output current $i_L(t)$; switching states $\mu(t)$. (b) System state controlled by standard MPC (0 < t < 1[ms]). (c) System state controlled as it is proposed (t > 1[ms]).

switching states in when a MPC strategy is applied to a FCC. Moreover, the switching states reduction proposed allows one not only to obtain a similar behavior than standard finite set control MPC but also to guarantee that system state will remain inside of a specific positive invariant set.

Even though the proposed strategy has been developed for constant current reference (dc-dc converter), we want to

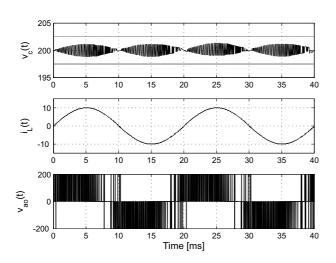


Fig. 7. Proposed MCP algorithm considering a sinusoidal current reference. Capacitor voltage $v_c(t)$; output current $i_L(t)$; output voltage $v_{an}(t)$.

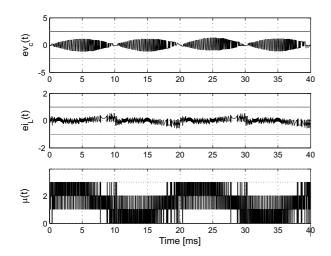


Fig. 8. Proposed MCP algorithm considering a sinusoidal current reference. Capacitor voltage error $ev_c(t)$; output current error $ei_L(t)$; switching states $\mu(t)$.

show the performance of this method when it is requered to track sinusoidal reference (dc-ac converter). Fig. 7 shows the result for this situation. The sinusoidal current reference $i_L^*[k]$ presents an amplitude of 10[A] and a frequency of $f_o = 50[Hz]$.

For this case, the admissible error region $\mathcal{D}[k]$ is now a variable set, but with respect to the origin $x[k] - x^*[k]$ is always the same. According to (24), to determine the worst case it is necessary to consider that in a instant k the system state is $x[k] = x^*[k]$. In this case the current reference is variable. However, the worst case among of all values that the output current can take is presented when the reference value is the sinusoidal peak. Taking this into account and keeping the sample frequency of $f_s = 20[kHz]$, the new de region \mathcal{D} referred to the origin is $\delta = [2.5 \ 1]^T$. In Fig. 8 one can see how the error is remained within the desired values using the proposed MPC algorithm.

VI. CONCLUSION

A strategy to reduce the number of switching states to be explored in a finite control state MPC has bee proposed. The most important benefits of this method is the good performance achieved in the tracking of the capacitor voltages and output current by exploring only those switching states which produce that the system states points towards the operating point. Due to this analysis is realized off-line, the time that the controller takes to find the optimal switching action to be applied is reduced. Other important fact is, when the references are constant, one can guarantee that the system state will remain inside of an invariant set determined by the allowable system error and the sample period. Moreover, capability of the proposed method for track sinusoidal current reference has been shown.

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