Predictive Control Algorithm Robustness for Achieving Fault Tolerance in Multicell Converters

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***Abstract*— Multilevel Converters (MCs) have emerged as a promising alternative to traditional two level converters. MCs use an arrangement of several semiconductors to synthesize high quality output voltage levels. Unfortunately, as a consequence of using more switching elements, MCs are, in general, more likely to be affected by faults, than their two level counterparts. In this paper, we propose a finite set constrained predictive control method for MCs, which is aimed at achieving robustness to failures in the semiconductors. We focus on three-phase multicell flying capacitor converters and show that, by carefully designing switching sequences, faults can be isolated from measurements provided by a single voltage sensor per phase. When faults occur, the proposed controller reconfigures the converter to provide to the load voltages which are similar to those obtained under normal, i.e., fault free, operating conditions.**

I. Introduction

Multilevel converters (MCs) have emerged as an important technology in many industrial applications. The main reason for this is that MCs are able to operate at far higher power levels and also provide output voltage and currents with lower distortion than their two level counterparts [1]. However, a major disadvantage of MCs is the increased probability of failure due to the larger number of devices required [2], [3].

In particular, flying capacitor converters (FCCs) have attracted significant attention [4]. As depicted in Fig. 1, FCCs are composed of multiple interconnected cells, which are composed by a capacitor C_x and a pair of switches S_{xi} and $\overline{S}_{xi}$, which work in complementary way. An internal short circuit occurs when a couple of complementary switches conducts at the same time, then the associated capacitor is forced to change its voltage, generating an increase of the current through it. Fortunately this fault currents decay quickly [2], since the associated capacitors seek voltage balance. These characteristics open the possibility to reconfigure the converter and continue its operation, albeit in general, at reduced performance level, as seen by the loads connected. To achieve robustness to failures, faults need to be isolated correctly and appropriate remedial actions must be taken quickly. Otherwise, additional faults will be triggered, leading to damages in the entire converter and, possibly, the load.

In [2], a fault detection strategy for multicell FCCs with switching patterns provided by open-loop PWM was proposed. Faults are detected in the frequency spectrum of the output voltage and the switching patterns are changed via shifting of the PWM carrier phases. Under fault conditions, the resultant output voltage waveform is synthesized with less levels. We can see that, whilst the method proposed in [2] gives some degree of robustness with respect to cell faults, performance is sacrificed significantly, when compared to normal operating conditions.

Recently, predictive control strategies [5] have been applied to power converters and multilevel converters in particular, see e.g. [6]–[10]. Advantages of using predictive control, when compared to traditional PWM methods, derive from the fact that changing operating conditions are explicitly accounted for. In addition, predictive control strategies allow one to not only control output currents, but also other aspects such as internal capacitor voltages and the switching [8], [9].

This paper presents a novel fault detection strategy for flying capacitor multilevel converters, which is based on predictive control. To allow the controller to detect internal short circuits and to determine which cell has failed, switch sequences are constrained to a reduced set. Whenever faults are detected, the proposed controller changes capacitor voltage references in order to keep the number of levels available for the output voltage. This reconfiguration method is then proposed which allows the converter to produce an output voltage characteristic, which is identical to that obtained under normal operating conditions.

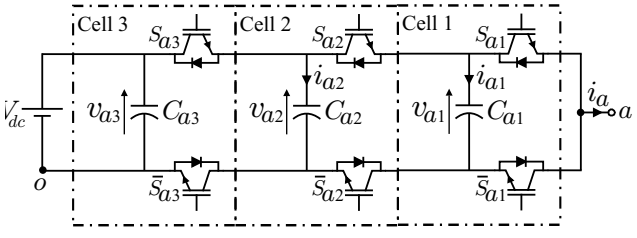

Fig. 1. Three-cell FC converter (phase a).

II. Flying Capacitor Converter

In this section we describe the flying capacitor topology in more detail and develop a model for the system.

A. Converter Model

In the present work, we will focus on an electrical system consisting of a 3 cell FCC connected to a coupled inductive load, as depicted in Fig. 2. The way in which the cells are connected, together with the capacitor voltages of each cell, determines the waveform output voltage synthesized.

Figure 1 shows a schematic of a single phase leg of a three-cell flying capacitor converter. As mentioned above, each cell consists of a capacitor and two switching elements which, at the same instant, cannot present the same state.

To characterize the output voltages of the three phase converter, we first note that, for phase a, we have:

$$v_{ao}(t) = v_{a1}(t)S_{a1}(t) + (v_{a2}(t) - v_{a1}(t))S_{a2}(t) + (V_{dc} - v_{a2}(t))S_{a3}(t), \quad (1)$$

The associated capacitor currents are

$$i_{a1}(t) = i_a(t)(S_{a2}(t) - S_{a1}(t)), \quad (2)$$
$$i_{a2}(t) = i_a(t)(S_{a3}(t) - S_{a2}(t)). \quad (3)$$

Table I shows the output voltages and currents for phase a, as a function of switch states.

The load voltages of the three phase converter are, thus, described via

$$\begin{bmatrix} v_{an}(t) \\ v_{bn}(t) \\ v_{cn}(t) \end{bmatrix} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix} \begin{bmatrix} v_{ao}(t) \\ v_{bo}(t) \\ v_{co}(t) \end{bmatrix} \quad (4)$$

A simple dynamic model of the system can be developed by noting this for one phase (in this case, the phase a) we have:

$$v_{a1}(t) = \frac{1}{C_{a1}} \int_{-\infty}^{t} i_{a1}(\tau)\, d\tau \quad (5)$$

$$v_{a2}(t) = \frac{1}{C_{a2}} \int_{-\infty}^{t} i_{a2}(\tau)\, d\tau \quad (6)$$

$$L\frac{di_a(t)}{dt} + Ri_a(t) = v_{an}(t), \quad (7)$$

$$v_{an}(t) = \frac{2}{3}v_{ao}(t) - \frac{1}{3}v_{bo}(t) - \frac{1}{3}v_{co}(t). \quad (8)$$

Similar equations are obtained for phases b and c.

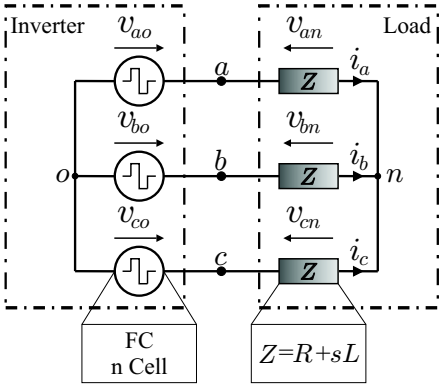

Fig. 2. Three phase FCC and load connection.

III. Fault Analysis in Flying Capacitor Converters

There are several kinds of failures that can occur in an FCC and many reasons causing them. Due to the large number of semiconductors which make up an FCC and the stresses to which they are exposed, switching failures in these converters are more likely than in their two-level counterparts.

The most common switch used in power converters is the Isolated Gate Bipolar Transistor (IGBT). Although, these elements can fail either short-circuit or open-circuit, open-circuit faults can be avoided by using an appropriated IGBT gate drive [2], [11]. Therefore, in the sequel we will concentrate on short-circuit faults.

A. Effects of a switch fault in a Flying Capacitor

In a FCC, a short circuited IGBT does not produce an abnormal output by itself. The fault only manifests itself once the complementary IGBT switches from OFF to ON. We call this a *cell fault*. Clearly, a cell fault can be produced only at a switching instant.

Depending on the cell which has failed, in a 3-cell FCC three different situations may arise. To elucidate this issue, in Fig. 3-a) a fault in cell 3 is shown (phase a). This fault causes the capacitor voltage v_{a2} to increase until it reaches the dc-link voltage V_{dc}. If the fault is produced in an internal cell, then the capacitor voltages at each side of the faulty IGBT are equalized to the average value before the fault. In the case of a 3-cell converter this would give v_{a2}=v_{a1}=$V_{dc}/2$, as shown in Fig. 3-b). Finally, Fig. 3-c) shows that a fault produced in the first cell forces this cell's capacitor to discharge completely, i.e. give v_{a1}=$0[V]$. The time taken to reach these capacitor

TABLE I

Switch states and output voltages of an FCC (phase a)

$S_a(S_{a3}, S_{a2}, S_{a1})$	$v_{ao}(t)$	$i_{a1}(t)$	$i_{a2}(t)$
$S_a(0,0,0) = 0$	0	0	0
$S_a(0,0,1) = 1$	$v_{a1}(t)$	$-i_a$	0
$S_a(0,1,0) = 2$	$v_{a2}(t) - v_{a1}(t)$	i_a	$-i_a(t)$
$S_a(0,1,1) = 3$	$v_{a2}(t)$	0	$-i_a(t)$
$S_a(1,0,0) = 4$	$V_{dc} - v_{a2}(t)$	0	$i_a(t)$
$S_a(1,0,1) = 5$	$V_{dc} - v_{a2}(t) + v_{a1}(t)$	$-i_a(t)$	$i_a(t)$
$S_a(1,1,0) = 6$	$V_{dc} - v_{a1}(t)$	$i_a(t)$	0
$S_a(0,0,0) = 7$	V_{dc}	0	0

TABLE II

OUTPUT VOLTAGES OF AN FCC UNDER A FAULT CONDITION (PHASE a)

$S_a = (S_{a3}, S_{a2}, S_{a1})$	$v_{ao}(t)$ in a Normal Condition	Failed Cell	$v_{ao}(t)$ in a Fault Condition
$S_a = (0,0,0) = 0$	0	Cell 1	0
		Cell 2	0
		Cell 3	0
$S_a = (0,0,1) = 1$	$v_{a1}(t)$	Cell 1	0
		Cell 2	$(v_{a2}(t) + v_{a1}(t))/2$
		Cell 3	$v_{a1}(t)$
$S_a = (0,1,0) = 2$	$v_{a2}(t) - v_{a1}(t)$	Cell 1	$v_{a2}(t)$
		Cell 2	0
		Cell 3	$V_{dc} - v_{a1}(t)$
$S_a = (0,1,1) = 3$	$v_{a2}(t)$	Cell 1	$v_{a2}(t)$
		Cell 2	$(v_{a2}(t) + v_{a1}(t))/2$
		Cell 3	V_{dc}
$S_a = (1,0,0) = 4$	$V_{dc} - v_{a2}(t)$	Cell 1	$V_{dc} - v_{a2}(t)$
		Cell 2	$V_{dc} - (v_{a2}(t) + v_{a1}(t))/2$
		Cell 3	0
$S_a = (1,0,1) = 5$	$V_{dc} - v_{a2}(t) + v_{a1}(t)$	Cell 1	$V_{dc} - v_{a2}(t)$
		Cell 2	V_{dc}
		Cell 3	$v_{a1}(t)$
$S_a = (1,1,0) = 6$	$V_{dc} - v_{a1}(t)$	Cell 1	V_{dc}
		Cell 2	$V_{dc} - (v_{a2}(t) + v_{a1}(t))/2$
		Cell 3	$V_{dc} - v_{a1}(t)$
$S_a = (1,1,1) = 7$	V_{dc}	Cell 1	V_{dc}
		Cell 2	V_{dc}
		Cell 3	V_{dc}

voltages depend on the capacitance values and the IGBT impedances and will in general be quick [2]. If the fault is not detected on time, fault repetitions will be produced in the cell, destroying the IGBT's [12] and the fault could be spread throughout the system.

B. Output Voltage Under a Fault Condition

As mentioned above, a cell fault can only be produced when a commutation is realized. These causes changes in one or two capacitor voltages e.g. v_{aj}, but not necessary in the output voltage v_{ao}. Table II shows how a cell fault will manifest itself in the output voltage v_{ao}, for a 3-cell FCC. Whether faults can be detected in the output voltages depends of the switch state and which cell is fault. For example, if the state S_a=3 is applied, then the output voltage will not be the expected one only if a fault is produced in cells 2 or 3. Conversely for this case, a fault in cell 1 is not perceived in the output voltage v_{ao}, because the expected and the observed output voltage are the same.

To make faults easily detectable from output voltage measurements, switching states sequences should be chosen as in Table III (the states for the other two phases are similar). These sets, namely $\mathcal{S}_a$, allow us to ensure that when a fault occurs, it will manifest itself in the output voltage, once a commutation is realized.

The only cases where the fault cannot be detected are when the states S_a=0 or S_a=7 are selected. However, in this situation a fault will always be detected at the next commutation instant. Consequently, we can always use the measurement of the output voltages v_{ao}, v_{bo}, v_{co} to identify a failed cell in one or, at most, two commutation instants.

IV. FAULT TOLERANT PREDICTIVE CONTROL STRATEGY

We can distinguish the following control objectives:

i. Tracking of three-phase output current references.
ii. Tracking of capacitors voltage references.

To achieve these objectives, even if a fault occurs, we will next present a predictive controller which minimizes a suitably defined cost function and where switching state sequences are restricted according to Table III (and similar sequences in the other two phases).

A. Basic Principles

The predictive control strategy is implemented in discrete time with sampling frequency $f_s = h^{-1}$. To obtain a discrete time model of the converter, we use a forward Euler approximation. Expression (1)-(8), then yields:

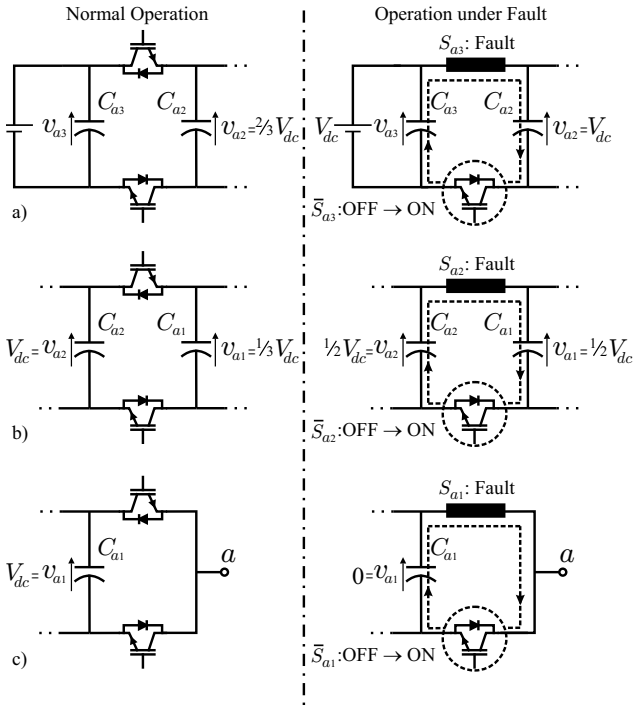

Fig. 3. Short Circuit in a FCC. a) Fault in Cell 3; b) Fault in Cell 2; c) Fault in Cell 1.

$$v_{ao}[k] = v_{a1}[k]S_{a1}[k] + (v_{a2}[k] - v_{a1}[k])S_{a2}[k] + (V_{dc} - v_{a2}[k])S_{a3}[k], \quad (9)$$

$$v_{a1}[k+1] = v_{a1}[k] + \frac{h}{C_{a1}}\left(S_{a2}[k] - S_{a1}[k]\right) i_a[k], \quad (10)$$

$$v_{a2}[k+1] = v_{a2}[k] + \frac{h}{C_{a2}}\left(S_{a3}[k] - S_{a2}[k]\right) i_a[k], \quad (11)$$

$$i_a[k+1] = \left(1 - \frac{hR}{L}\right) i_a[k] + \frac{h}{L} v_{an}[k], \quad (12)$$

$$v_{an}[k] = \frac{2}{3} v_{ao}[k] - \frac{1}{3} v_{bo}[k] - \frac{1}{3} v_{co}[k]. \quad (13)$$

where $x[k] \triangleq x(kh)$.

To incorporate the tracking objectives (i.) and (ii.), we define the error signals per phase via:

$$e_y[k] \triangleq \begin{bmatrix} v_{y1}[k] - v_{y1}^*[k] \\ v_{y2}[k] - v_{y2}^*[k] \\ i_y[k] - i_y^*[k] \end{bmatrix}, \quad y \in \{a, b, c\} \quad (14)$$

where $i_y^*[k]$ are the desired three phase sinusoidal current references.

Under normal fault-free operating conditions, so-called "balanced" capacitor voltage references are chosen [13],

$$v_{y1}^*[k] = \frac{V_{dc}}{3}$$
$$v_{y2}^*[k] = \frac{2V_{dc}}{3}$$

If a *cell fault* is detected, then the capacitor voltage reference of the associated phase is changed to keep normal output voltage levels, despite the fault conditions [14].

At each time instant k, a measurement of the capacitor voltages and load currents is used for the minimization of the following cost function:

$$J(S_a, S_b, S_c)[k] = \sum_{y \in \{a,b,c\}} e_y[l]^T P e_y[l] \quad (15)$$

where

$$P = diag\{\lambda_1, \lambda_2, 1\} \quad (16)$$

Here, λ_1 and λ_2 are design parameters, which allow one to trade current tracking errors versus capacitor voltage tracking errors and, thus, achieve the proposed goals (i) and (ii). The decision variables are S_a, S_b and S_c, which are restricted to belong to the finite sets defined in Table III, to allow the fastest fault detection.

The optimal switching action to be applied at time $k+1$, namely $S_{opt}[k]$ is obtained by minimizing $J(S_a, S_b, S_c)[k]$. Then, at the next sample time, $k+1$, the cost function $J(S_a, S_b, S_c)[k+1]$ is minimized using fresh state measurements. This gives $S_{opt}[k+1]$, etc.

As will be apparent in Section V, this control method gives robust performance of the converter, as seen by the load. Consequently, the FCC does not need to be shut down immediately, but can be repaired when convenient.

TABLE III
SET OF SWITCHING STATES DEPENDING OF THE PREVIOUS STATE (PHASE A)

$S_a(k-1)$	$S_a(k)$
0	$\{0, 1, 2, 4\}$
1	$\{0, 1, 2, 3, 5\}$
2	$\{0, 1, 2, 4, 7\}$
3	$\{1, 2, 3, 5, 7\}$
4	$\{0, 2, 4, 5, 6\}$
5	$\{0, 3, 5, 6, 7\}$
6	$\{2, 4, 5, 6, 7\}$
7	$\{3, 5, 6, 7\}$

B. Estimation of Capacitor Voltages using Output Voltage Feedback

The predictive controller proposed in the previous section, in principle requires 3 sensors per phase when applied to a 3-cell FCC [8]. They are 2 measurements of the capacitor voltages and one of the output current. In addition, we also require measuring the output voltages v_{ao}, v_{bo}, v_{co} to identify a possible cell fault. More generally, in a three-phase n-cell FCC the number of sensors would be $3(n+1)$. To reduce the number of sensors needed, we estimate the capacitor voltages from (5)-(6), which in discrete time can be rewritten via:

$$v_{y1}[k] = v_{y1}[k-1] + \frac{h}{C_{y1}}(S_{y2}[k-1] - S_{y1}[k-1]) i_y[k]$$
$$v_{y2}[k] = v_{y1}[k-1] + \frac{h}{C_{y2}}(S_{y3}[k-1] - S_{y2}[k-1]) i_y[k]$$

where $i_y[k]$, $y \in \{a, b, c\}$ refers to the current values.

In a real implementation, this rather simple approach can produce an incremental error due to inaccuracy of the model used, e.g., dead time, saturation volt drop and capacitors tolerance. To improve this situation, estimates can be corrected by measuring, at some instants the capacitor voltages. For that propose, one can simply utilize the output voltage measurement whenever the applied state is $S_a(t)$=1 or $S_a(t)$=3. The output voltage will be $v_{ao}(t)$=$v_{a1}(t)$ or $v_{ao}(t)$=$v_{a2}(t)$, respectively. The above method allows one to reduce the number of sensors, using only one measurement of voltage per phase to determine the internal values of the capacitor voltages and to detect a fault condition. This is especially useful for a large number of cells.

V. RESULTS

To verify the performance of the proposed strategy, simulation studies were carried out on a three-phase with three cells per phase. A main dc-link voltage of V_{dc}=300$[V]$ was used. The electrical parameters were: C_{yj}=470$[\mu F]$, R=2.5$[\Omega]$ and L=1$[mH]$. The three phase current references i_y^* have an amplitude of $50[A]$ and a frequency of f_o=50$[Hz]$.

These simulations consisted of exposing the converter to an internal fault. The performance of the converter operating with the proposed method is compared with the standard predictive control applied under the same conditions. Additionally, the proposed scheme was compared to standard PWM reconfiguration.

A. Standard Predictive Control

Standard predictive control was applied using a sample frequency of f_s=25$[kHz]$. Furthermore, the controller is adjusted using weight factors λ_1=λ_2=0.1. In this case, the state $S_y[k]$ does not depend of his previous state $S_y[k-1]$. The results of this simulation are presented in Fig. 4. It is possible to see from the figure that the controller achieved good performance in the three phase currents and the capacitors voltage. At time t=51.48$[ms]$ switch S_{a2} is kept in a permanent ON state simulating a short circuit failure of the switch. Then a *cell fault* occurs every time that switch $\bar{S}_{a2}$ commutates to an ON state, therefore, the *cell fault* is not always present. In this case the capacitor voltages v_{a1} and v_{a2} are equalized, reaching a value of $V_{dc}/2$. This causes a reduction in the number of levels in the output voltage $v_{ao}(t)$. Other consequence can be noted in the capacitor voltages behavior, the controller does not know cell 2 has failed, affecting cell 1 in the process, and tries to control them, it reduces the performance in the output voltage $v_{ao}(t)$ and in the line to line voltage $v_{ab}(t)$. This behavior could be detrimental to the converter itself causing a succession of faults and eventually catastrophic failure [12].

B. Fault Tolerant Strategy

We next examine the algorithm proposed in Sec. IV. In this case, the capacitor voltages are estimated using output voltage feedback and switching states are restricted according Table III. As can be seen in Fig. 5, startup is similar to

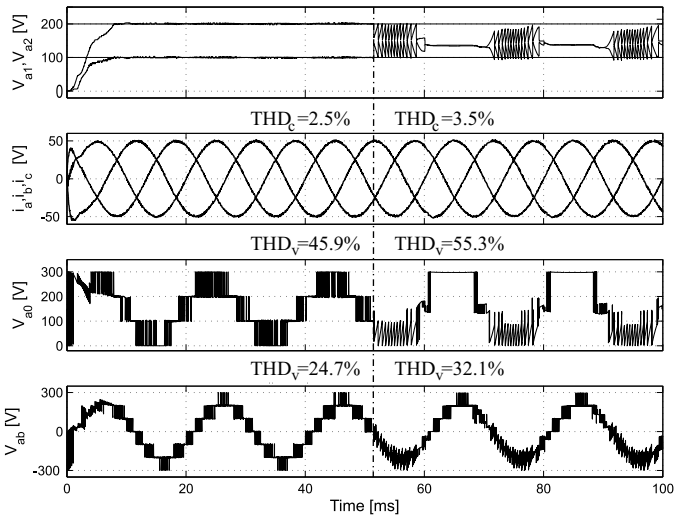

Fig. 4. Standard predictive control strategy, λ_1=λ_2=0.1: capacitors voltages v_{a1},v_{a2}, load currents i_a, i_b, i_c, output voltage v_{ao} and corresponding line to line voltage v_{ab}.

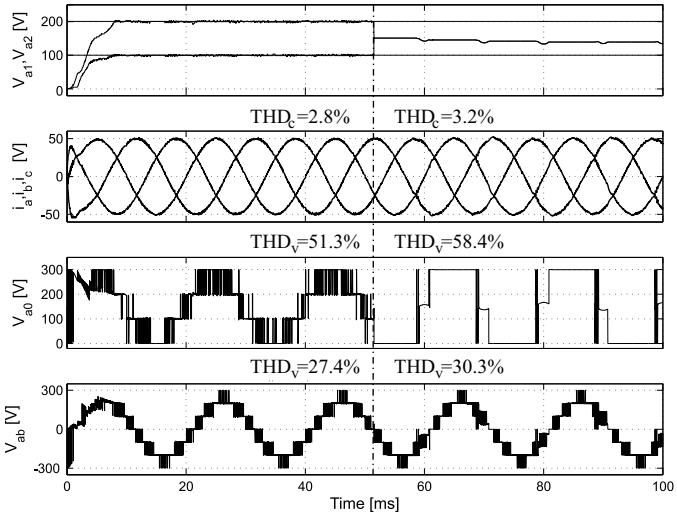

Fig. 5. Predictive control robustness to fault, λ_1=λ_2=0.1: capacitors voltages v_{a1},v_{a2}, load currents i_a, i_b, i_c, output voltage v_{ao} and corresponding line to line voltage v_{ab}.

the *standard predictive control*. It is possible to see, in a fault free condition, the electrical variables have a distortion slight higher than the standard method. This is because of the reduced set of permitted switch state sequences. When the fault is produced, the capacitor voltages are equalized, but in this case the fault is detected and then the cell is isolated and is discarded in the optimization. Therefore, the line to line voltage $v_{ab}(t)$ presents a better behavior (THDv=30.3%) than in the standard predictive control (THDv=32.1%).

C. Standard phase shifted PWM with Fault Reconfiguration

To analyze the reconfiguration performance, we next study the method proposed in [2], which uses phase shifted PWM modulation. This method achieves reconfiguration by changing the phase of the carrier in order to obtain a three level output

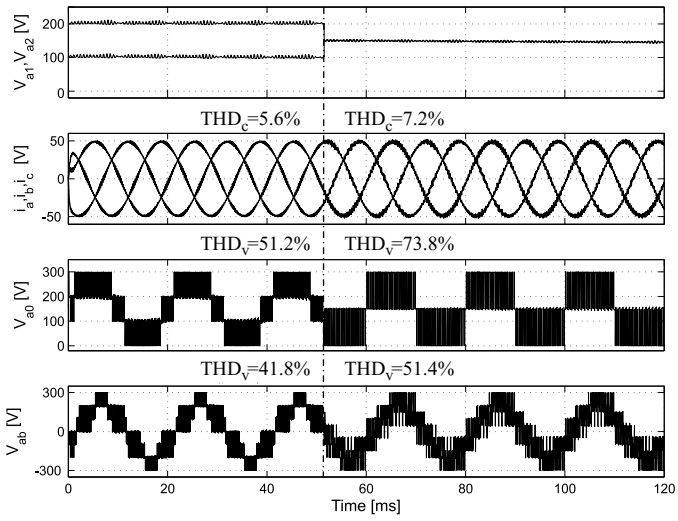

Fig. 6. Standard phase shift PWM with reconfiguration, f_c=4.5$[kHz]$: capacitors voltages v_{a1},v_{a2}, load currents i_a, i_b, i_c, output voltage v_{ao} and corresponding line to line voltage v_{ab}.

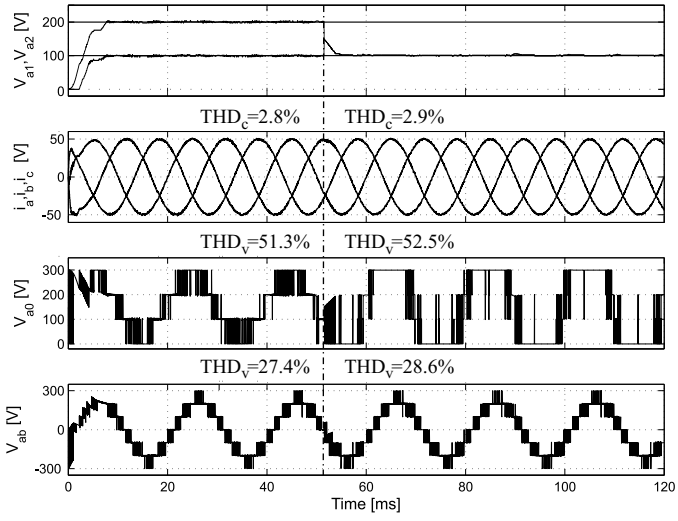

Fig. 7. Predictive control robustness to fault with reconfiguration, λ_1=λ_2=0.1: capacitors voltages v_{a1},v_{a2}, load currents i_a, i_b, i_c, output voltage v_{ao} and corresponding line to line voltage v_{ab}.

voltage.

In the simulation, the carrier frequency selected per cell is f_{cc}=1.5$[kHz]$, obtaining a switching output voltage of f_c=4.5$[kHz]$. In Fig. 6, the result of the same fault case as considered previously is shown. (Note, that startup performance was not included in this simulation due to it takes a long time using PWM [8] and it is not the focus of this work.) This strategy improves the output voltage of the phase that has failed but does not achieve good results with respect to the line to line voltage.

D. Predictive Control Robustness to Faults with Reconfiguration

In this case, a change in the reference of the capacitor voltages is proposed as a reconfiguration method. Figure 7 shows

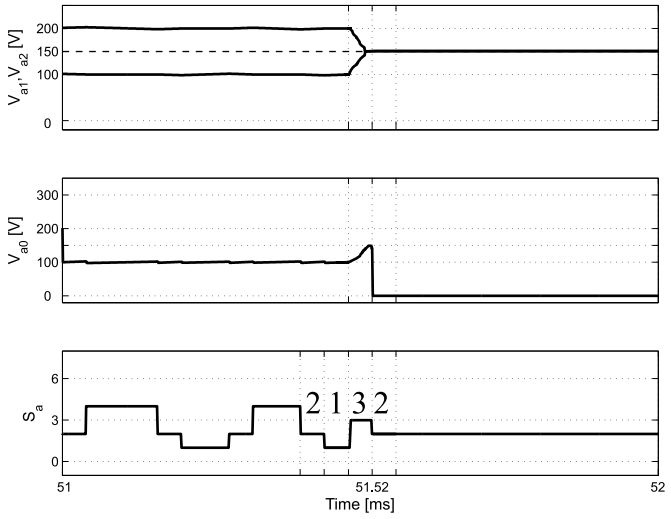

Fig. 8. Predictive control robustness to fault with reconfiguration, λ_1=λ_2=0.1: capacitors voltages v_{a1},v_{a2}, output voltage v_{ao} and corresponding switch sequence applied S_a.

the results from the fault case considered in the previous three simulation studies. When the fault occurs (at $t \approx 51.48[ms]$), the phase output voltage loses a level. In this case, under fault, v_{a1} and v_{a2} works as a unique capacitor, then phase a operates as a 2-cell FCC. So, as proposed in [14], the number of levels can be increased by changing the capacitors voltage ratio. Thus, the equivalent capacitor between C_{a1} y C_{a2} is forced to take a voltage of $V_{dc}/3$, restoring the fourth level in the output voltage v_{ao}. Moreover, the increase in the distortion in the electrical variables, under a fault condition, is clearly less than in the other cases studied, keeping a good performance in both situations.

Finally, a zoom of the fault instant is presented in Fig. 8. In this figure it is possible to see how the state S_a follows a permitted sequence according to Table. III. In addition, the reader should note that the fault occurs when the state S_a changes from $S_a(0,0,1)$=1 to $S_a(0,1,1)$=3. Under normal operating conditions the expected value of the output voltage is v_{ao}=v_{a2}=200$[V]$, but the measured output voltage is v_{ao}=150$[V]$. Inspection of Table II tells us that a fault in cell 2 has occurred.

VI. Conclusion

A Predictive Control strategy to achieve robustness to faults has been proposed. This methodology is applied to a three phase 3-cell FCC. The most important benefits of this method is the good performance achieved in the tracking of the capacitor voltages and the three phase currents even when a fault occurs. The fault is identified using the measurement of the output voltages. To ensure the fault be detected quickly, switching sequences are restricted to a reduced set.

We also showed how to estimate the capacitors voltages from output voltage measurements, thus reducing the number of sensors needed for implementation. The authors consider that the strategy proposed expands the possibilities of the

predictive control in industrial application not only to achieve good performance in the tracking errors but also to accelerate the fault time detection.

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