Comparison of Modulation Strategies for a Cascaded H-bridge StatCom - Part 2: Application of the Analysis

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***Abstract*—A companion paper provided the theoretical basis for a comparison between phase shifted carrier and space vector modulation schemes [1]. This paper utilises the analysis techniques developed to investigate some non-ideal implementation aspects of the modulation strategies as well as the effect of increasing the level number on the performance of the cascaded H-bridge static compensator (H-StatCom). Specifically, non-ideal elements of the modulation scheme, such as non-uniform DC bus voltages, carrier phase-shift error and transient capacitor voltages are discussed. Simulation results are presented which show that there is an important relationship between the performance of the phase shifted carrier technique and the number of levels in the H-StatCom.**

I. Introduction

The Cascaded H-bridge multi-level converter is becoming a popular topology for multi-level Static Compensators (StatComs). There are a number of reasons for this, but the main one is that it is feasible to obtain a large number of levels with this topology [2]. With alternative topologies the level numbers are constrained by component number and capacitor voltage balance issues [3], [4]. The other important advantage of the H-bridge multi-level converter is that the topology is ideally suited to reactive power and harmonic filtering applications as the converter does not need to handle any real power, and therefore there is no need for expensive isolated DC power supplies [5]. Also, the increased number of levels achievable with the topology allows greater switching redundancy, which creates more flexibility in terms of harmonic performance, switching losses and voltage balancing. This is an important point in the context of the comparison between the performance of the PSC-PWM and SVM schemes, and is expanded upon within this paper.

A companion paper [1] developed mathematical expressions to allow the investigation of the effects on the harmonic performance of PSC-PWM due to non-ideal DC bus voltages, phase-shift error and transient capacitor voltages. The analysis can be used to form the basis for an effective comparison between modulation strategies. In this paper the analysis is applied to a particular H-StatCom with a typical operational condition. The analysis is also extended to consider the important effect of varying the output current and level number on the harmonic performance of the H-StatCom. The analysis is confirmed through simulation studies.

Space Vector Modulation is an alternative modulation scheme used to calculate appropriate switching instants without relying on comparison operations between reference and carrier waveforms. The use of SVM in a H-StatCom application creates an extra degree of freedom, which can be used to create an effective voltage balancing scheme [6]. This balancing scheme avoids the control loop interactions present in the technique described in [7]. With this advantage of SVM in mind, the paper makes a comparison between PSC-PWM and SVM in terms of harmonic performance and switching frequency. It is shown there is a point at which the harmonic performance trade-off with the switching losses is similar for both techniques, and with the ease of implementation of SVM it is proposed that this technique will begin to gain wider acceptance for use in H-StatComs above a certain level number.

II. Application of analysis to an 11kV H-StatCom

To apply the analysis developed in Part 1 of this paper the H-StatCom application and operational condition must be defined. The authors have attempted to consider a typical application with common operational goals and common limitations encountered in the design of H-StatCom systems. The rationale behind the choice of these parameters is discussed in Part 1 of this paper. The H-StatCom application is defined as follows:

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- H-StatCom is rated as 11kV_{l-l} direct connect;
- It has 19-levels, and consists of nine H-bridges per phase-leg;
- The peak leading current is $100A$;
- A nominal bridge capacitance of $2200\mu F$. The authors believe a choice of $2200\mu F$ is reasonable for an 11kV_{l-l} direct connected H-StatCom based on capacitor cost and space requirements;
- With nominal capacitance of $2200\mu F$ and a 9 bridge stack the corresponding bridge capacitance values are distributed as follows: $C_1 = 2090\mu F$, $C_2 = 2131\mu F$, $C_3 = 2172\mu F$, $C_4 = 2213\mu F$, $C_5 = 2255\mu F$, $C_6 = 2296\mu F$, $C_7 = 2338\mu F$, $C_8 = 2379\mu F$, $C_9 = 2420\mu F$;
- A nominal value of 10mH for the H-StatCom connection inductance.

To establish the deterioration in harmonic performance due to the non-uniform DC bus voltages it is necessary to calculate the variance in the capacitor voltages for this application. By modifying the capacitance value in (1) it is possible to determine the variance in capacitor voltage ripple for nine H-bridges with capacitances given above. Note that (1) was developed in Part 1 of this paper.

$$V_C(t) = \left(\frac{A^2 V_m^2}{N_C^2} + \frac{V_m I_m}{2\omega N_C C} \left[\sin(2\omega t + \varphi) - \sin\varphi \right] + \frac{V_m I_m}{N_C C}\, t\, \cos\varphi \right)^{\frac{1}{2}} \quad (1)$$

Fig. 1 shows the resultant voltage waveforms, at the peak of the waveform there is a voltage difference of $6V$. To utilise (2), which was developed in Part 1 of this paper, we can assume an average value for the difference in DC bus voltage. This is done by calculating the RMS voltage for each of the bridge capacitors. The resultant values for V_{dc} are: $V_{dc\,1} = 1479.61$, $V_{dc\,2} = 1480.05$, $V_{dc\,3} = 1480.49$, $V_{dc\,4} = 1480.93$, $V_{dc\,5} = 1481.37$, $V_{dc\,6} = 1481.82$, $V_{dc\,7} = 1482.26$, $V_{dc\,8} = 1482.70$, $V_{dc\,9} = 1483.14$.

$$\begin{aligned} &V_{dc\,1} \cos\left(2m \left(\omega_c t + \frac{[1-1]\,\pi}{N} \right) + [2n-1]\, 2\omega_o t \right) \\ &+ V_{dc\,2} \cos\left(2m \left(\omega_c t + \frac{[2-1]\,\pi}{N} \right) + [2n-1]\, 2\omega_o t \right) \\ &+ \ldots + V_{dc\,N} \cos\left(2m \left(\omega_c t + \frac{[N-1]\,\pi}{N} \right) + [2n-1]\, 2\omega_o t \right) \end{aligned} \quad (2)$$

Fig. 2 shows the resultant Fourier spectrum when evaluating (2) for the listed DC bus voltages. It is important to note that

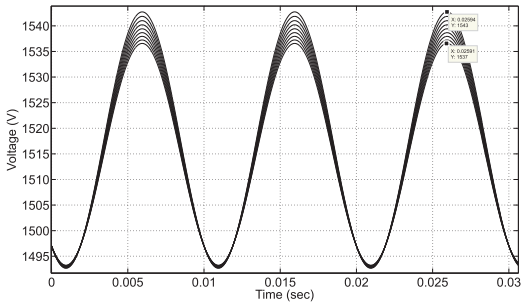

Figure 1. Theoretical Capacitor Voltage Ripple for an 11kV_{l-l}, 9-bridge H-StatCom supplying a peak leading current of 100Amp.

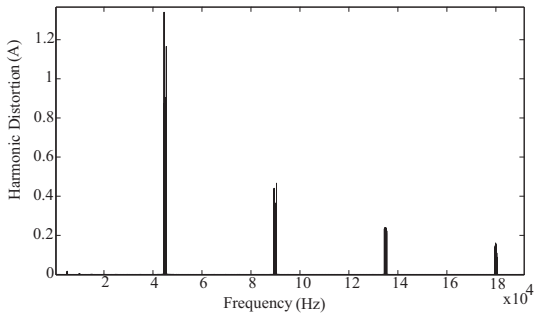

Figure 2. Fourier spectrum of the practical implementation of the PSC-PWM scheme for the range $0 \rightarrow 180\text{kHz}$

Fig. 2 gives us a measure of the harmonic coefficients for this practical implementation of a H-StatCom. Fig. 3 shows a close up of Fig. 2 for the frequency interval $0 \rightarrow 40\text{kHz}$. The harmonics introduced in this interval are a consequence of the capacitor voltage ripple, and only arise in the practical implementation of a H-StatCom. The magnitude of these harmonics are relatively small when compared to the harmonic peaks at $2N$. However they have an effect on the harmonic spectrum of the resultant H-StatCom current, because of their relatively low frequency. For this example it was calculated that by modeling the capacitor voltage ripple the Total Harmonic Distortion (THD) of the output current increases from 0.00247 to 0.00248. Therefore for this particular operational condition the harmonic deterioration is very minor.

It is useful at this point to quantify the harmonic performance of the equivalent SVM scheme. Fig. 4 shows the harmonic spectrum for the SVM scheme for the same operational condition as the preceding PSC-PWM analysis. The associated THD for the current spectrum was calculated at 0.0287. This is an order of magnitude larger than the THD associated with the PSC-PWM scheme.

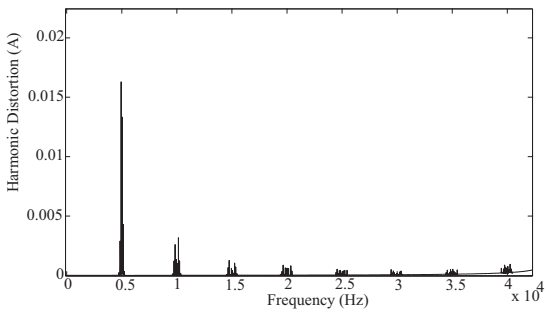

Figure 3. Fourier spectrum of the practical implementation of the PSC-PWM scheme for the range $0 \rightarrow 40$kHz

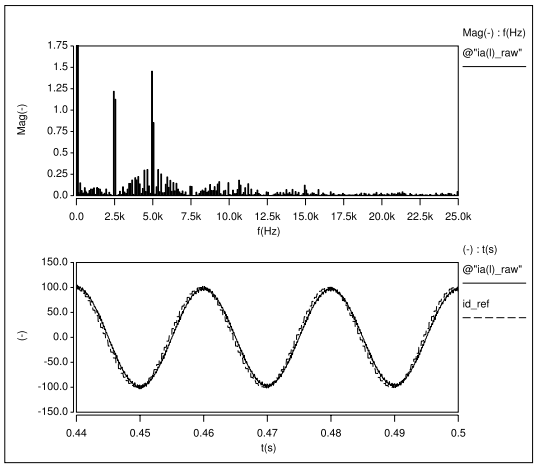

Figure 4. Fourier Spectrum of the SVM Scheme

Having calculated the harmonic performance of both the PSC-PWM and SVM schemes, it is now possible to investigate the trade-off between harmonic performance and switching losses for each scheme. This can be done in various ways however many commercial H-StatComs use the switching frequency per component as the basis for their design choice [8]. For PSC-PWM each switching device will undergo two switching transitions per period of the carrier waveform, this is due to the fact that PSC-PWM switches in each bridge during every period of the carrier waveform. To calculate the switching transitions for a SVM scheme such as [6] is more difficult due to the variable nature of the switching. Section IV investigates the possible reduction in switching transitions which can be achieved using the SVM scheme. This analysis shows that for the considered operational condition the switching frequency per component is approximately three times less than that of PSC-PWM for a 19-level H-StatCom.

Clearly for the operational condition analysed the trade-off between harmonic performance and switching losses, the PSC-PWM scheme is clearly superior. For this condition the THD is more than ten times less than that of the SVM scheme with three times the number of switching transitions per component. However, as will be shown in Section IV, the analysis can be extended to include higher level numbers where the benefits of PSC-PWM are not so obvious.

III. The effect of H-StatCom Output Current

The H-StatCom output current will have an important effect on the harmonic performance due to the relationship between the current and capacitor voltage ripple. It is useful to analyse this relationship for the PSC-PWM and SVM implementations so that any effect on the harmonic performance can be quantified.

For every control interval, PSC-PWM switches each bridge in the stack, while SVM makes some logical choice as to which bridges will be used to create the voltage waveform. If the H-StatCom is supplying lagging VARs then the RMS magnitude of the H-StatCom voltage will be less than that of the network voltage. Under this condition when the stack is modulated using PSC-PWM, the required pulse widths will be smaller than those required when supplying leading VARS. So for the same magnitude H-StatCom current, the capacitors will experience a smaller voltage ripple when supplying lagging VARS.

When the bridges are modulated using SVM the capacitor voltage ripple will manifest itself in a different way. For example, when supplying lagging VARS the H-StatCom output voltage will be smaller and therefore less bridges will be switched in for a given control period, as compared to the case of supplying leading VARS. However because the bridges will be switched in for the entire control interval they will experience a greater change in voltage for the same output current, as compared to when PSC-PWM is employed. Essentially this discussion underlines the fact that PSC-PWM more evenly shares the voltage ripple through the stack in any one control interval. When looking at the complete fundamental period however the ripple will be similar regardless of modulation strategy.

When there is an increase in the time that the bridges are switched in, the greater the difference in voltage ripple between bridges of differing capacitance and, as shown, the less effective the PSC-PWM harmonic cancellation is. The analysis for the condition of supplying leading VARS produced results that indicate degraded harmonic performance for PSC-PWM, more-so than when supplying lagging VARS. This relationship is depicted in Fig. 5 which is an evaluation of (1) showing the variance in capacitor voltage ripple as a function of H-StatCom RMS voltage.

The graph can be divided into two sections. When the H-StatCom voltage is larger than that of the system voltage the

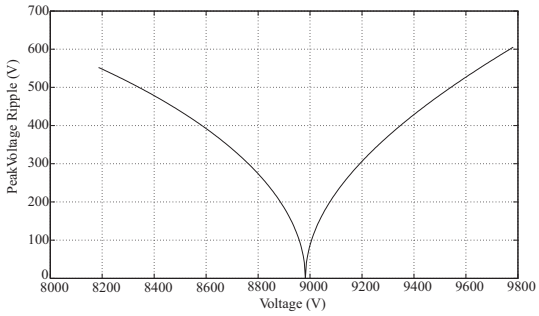

Figure 5. Capacitor voltage ripple as a function of H-StatCom RMS Voltage

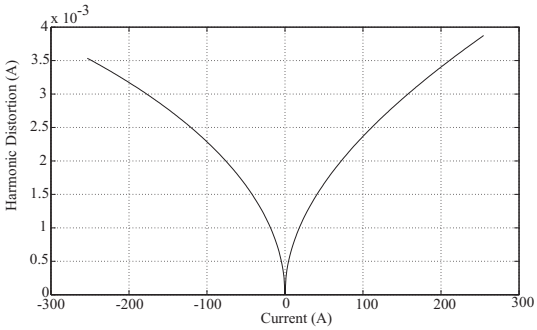

Figure 6. Harmonic Distortion at $5kHz$ as a function of H-StatCom Current

H-StatCom is supplying leading VARS. For this condition the voltage ripple increases more rapidly than when supplying lagging VARS because in the lagging case the increase in effective pulse width is being balanced out by the fact that the current magnitude is decreasing. In the leading VAR case the capacitor voltage ripple increases more rapidly because both the current magnitude and effective pulse widths are increasing. It can be argued that most StatComs will usually be supplying leading VARS to compensate for the inductive nature of the majority of industrial and domestic loads. However, for the sake of completeness, the proceeding analysis and simulations will present results for both leading and lagging conditions.

Having established the variation in capacitor voltage ripple for varying H-StatCom currents, it is possible to calculate the harmonic distortion due to these voltage ripples by evaluating (2). Fig. 6 shows the harmonic distortion associated with the second order carrier waveform i.e. in this case the harmonics centered at $5\mathrm{kHz}$. The graph has an identical shape to that of Fig. 5, as expected given that there is a linear relationship between capacitor voltage ripple and the subsequent harmonic distortion, when the deviation in capacitance remains constant.

IV. Increasing the H-StatCom Level Number

This section will show that there is an important relationship between the harmonic performance of the phase shifted carrier technique and the level number of the H-StatCom. The analysis is restricted to the situation where practical implementation errors remain constant with increasing level number. For this condition, the resultant waveforms show that the summation of harmonics between the H-bridges in each stack leads to an increasing current THD. With this in mind, it is possible to find a point at which the harmonic performance trade-off with the switching frequency becomes comparable to that of the space vector modulation technique. The variation of this point is investigated for various operational conditions and implementation errors.

Firstly, harmonic performance and switching losses for the SVM scheme are calculated, through simulation, as a function of level number. Then the deterioration of the harmonic performance of PSC-PWM is investigated to find the cross-over point at which the performance of SVM becomes comparable.

Fig. 7 shows the dependency of switching frequency on the level number, when SVM is being employed in a H-StatCom. This graph shows that with an increasing level number the switching frequency per component decreases asymptotically. This is due to the extra redundancy in a higher level number H-StatCom which decreases the likelihood for a particular bridge to be switched in for a given control cycle. This is due to an increase in available stack voltage in comparison to the constant voltage difference which is required across the H-StatCom inductance to create the same current.

Fig. 7 was produced through Matlab simulation which implements the control scheme in [6], for the operational condition described in [1]. Note that Fig. 7 was produced using a constant H-StatCom current. There will be some variation to the shape of the curve for varying currents due to the change in RMS stack voltage required to affect the change in current. This variation is small, particularly for higher level numbers where the change in RMS stack voltage is relatively small.

The harmonic performance of SVM will not vary with the increase in level number, when the H-StatCom is in a constant operational state i.e. the voltage rating and H-StatCom output current remain constant. This is because the voltage waveform will be identical regardless of level number. There will be a greater number of bridges that are available to create the voltage waveforms, but the control strategy described in [6] will ensure that the same voltage will be created for each control cycle, and therefore the harmonic content of the waveform will be identical. This phenomenon is a consequence of the SVM scheme only PWM'ing one bridge in the phase-leg, regardless of how many bridges the leg consists of.

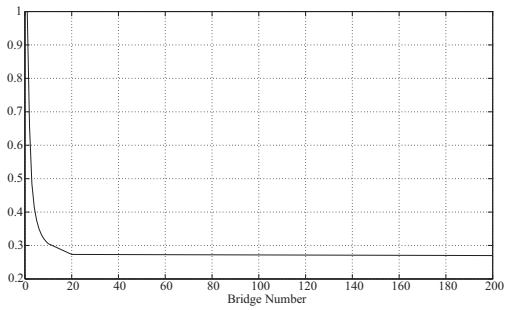

Figure 7. Switching frequency of one H-bridge relative to control frequency

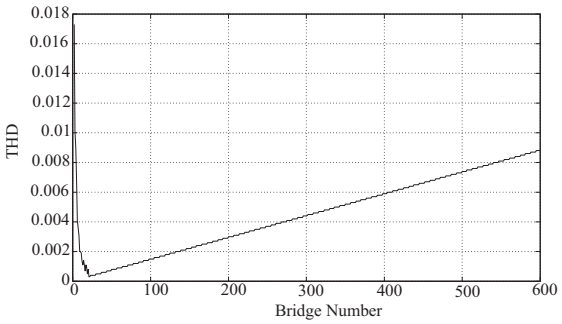

Figure 8. THD for the H-StatCom current for an increasing bridge number with only non-ideal DC capacitor voltages

Fig. 8 depicts the harmonic performance of PSC-PWM as the level number increases, under the assumption of the same operational condition. This graph is produced by evaluating (2) for increasing N values.

By comparing Figs. 7 and 8 and using (3), it is possible to determine the point at which the harmonic performance and switching loss trade-off crosses over.

$$\mathrm{THD}_{\mathrm{SVM}} \times f_{sw\,SVM} = z = \mathrm{THD}_{\mathrm{PSC}} \times f_{sw\,PSC} \qquad (3)$$

When $N = 270$ the harmonic distortion of the PSC-PWM scheme is 0.004, but for $N = 270$ the switching frequency per component of the SVM has reduced to 0.28. As mentioned previously, for PSC-PWM each switching component will undergo two switching transitions each control period therefore $f_{sw\,PSC} = 2$. So via (3), $N = 270$ is the cross-over point. While this cross-over point is very high it is important to note that there is a linear relationship between capacitance deviation, magnitude of the H-StatCom current and the THD of the resultant current. Therefore the cross-over point can be significantly lower if the deviation and/or the current magnitude is larger.

The mathematical descriptions for the PSC-PWM waveforms assume that the phase-shifts applied to the carriers are ideal. In practice there will be some small but finite error in these shifts due to the digital to analog interface within the modulation scheme. This error is difficult to quantify however this paper provides some qualitative discussion on the importance of considering this effect in terms of the harmonic performance. This is achieved by using the mathematical description of the resultant waveforms under the condition of a typical error in the carrier phase-shifts.This description was developed in Part 1 of this paper and is shown in (4).

$$\begin{aligned}\cos\left(2m\left(\omega_c t + \frac{[1-1]\,\pi}{N}\right) + \theta_1 + [2n-1]\,2\omega_o t\right) \\ + \cos\left(2m\left(\omega_c t + \frac{[2-1]\,\pi}{N}\right) + \theta_2 + [2n-1]\,2\omega_o t\right) \\ + \ldots + \cos\left(2m\left(\omega_c t + \frac{[N-1]\,\pi}{N}\right) + \right. \\ \left. \theta_N + [2n-1]\,2\omega_o t\right) \qquad (4)\end{aligned}$$

The cross-over point is further reduced when the phase-shifts of the carrier waveforms is considered. This example assumes the variance in phase error is distributed linearly through the stack i.e. with a error of $\pm 1^\circ$ and a 9 bridge stack the corresponding θ values are as follows: $\theta_1 = -1^\circ$, $\theta_2 = -0.75^\circ$, $\theta_3 = -0.5^\circ$, $\theta_4 = -0.25^\circ$, $\theta_5 = 0^\circ$, $\theta_6 = +0.25^\circ$, $\theta_7 = +0.5^\circ$, $\theta_8 = +0.75^\circ$, $\theta_9 = +1^\circ$.

Fig. 9 was produced by evaluating (4) for increasing N. It can be calculated that the cross-over point has further reduced to $N = 35$. Even though this indicates that the harmonic performance of PSC-PWM is clearly superior to SVM for all practical numbers of bridges , the analysis nevertheless does demonstrate the importance of the phase-shift accuracy, and the effect that it can have on the harmonic performance. What is also of importance is the sensitivity of the distortion to varying phase-shift error. Fig. 10 shows the harmonic distortion associated with the second order carrier waveform i.e. in this case the harmonics centered at 5kHz, as a function of phase-shift error. It can be seen that the increase in distortion has a linear relationship to the amount of deviation in phase-shifts between the bridges.

In the preceeding discussion it was assumed that the H-StatCom was in a steady state operational condition implying that the individual capacitor voltages are inherently balanced over the fundamental period. In this section the transient condition is considered which includes the modification of the H-bridge references due to the voltage balancing scheme. Again it is difficult to quantify the necessary modification to the

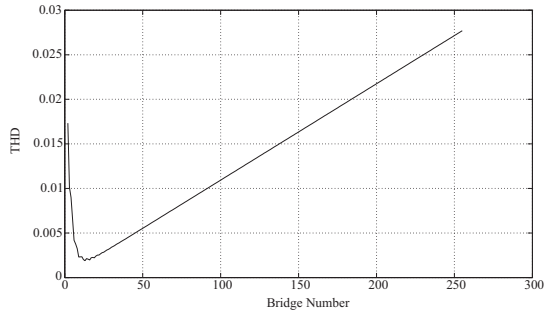

Figure 9. THD for the H-StatCom current for an increasing bridge number with non-uniform DC bus voltages and phase-shift error included

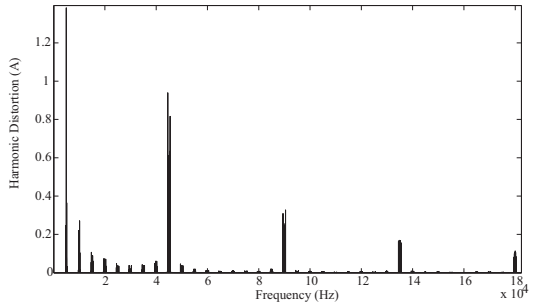

Figure 11. Fourier Spectrum for the PSC-PWM scheme with transient capacitor voltages

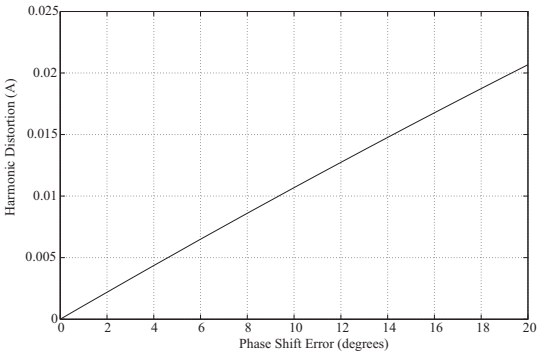

Figure 10. Distortion introduced at $5kHz$ by an increasing phase-shift error

references to achieve capacitor voltage balancing, however some qualitative discussion is provided to outline the importance of this effect. This is achieved by using the mathematical description of the resultant waveforms under the condition of a typical transient condition. This description was developed in Part 1 of this paper and is shown in (5) below.

$$\hat{V}_{\mathrm{bridge}_1}\cos\left(2m\left(\omega_c t+\frac{[1-1]\,\pi}{N}\right)+[2n-1]\,2\omega_o t+\theta_1\right)+\hat{V}_{\mathrm{bridge}_2}\cos\left(2m\left(\omega_c t+\frac{[2-1]\,\pi}{N}\right)+[2n-1]\,2\omega_o t+\theta_2\right)+\ldots+\hat{V}_{\mathrm{bridge}_N}\cos\left(2m\left(\omega_c t+\frac{[N-1]\,\pi}{N}\right)+[2n-1]\,2\omega_o t+\theta_N\right) \quad (5)$$

As an example the analysis will assume that the average capacitor voltages are equal up to a particular fundamental period, after which there is a variance in the average voltages. We will assume a variance of $\pm 30V$ over the fundamental period which will give the following V_i values $V_1 = 1479.61$, $V_2 = 1483.36$, $V_3 = 1487.11$, $V_4 = 1490.86$, $V_5 = 1494.61$, $V_6 = 1498.36$, $V_7 = 1502.11$, $V_8 = 1505.86$, $V_9 = 1509.61$.

Fig. 11 shows the harmonic spectrum produced by evaluating expression (5), for an $11\mathrm{kV}_{l-l}$ H-StatCom producing a peak leading current of $100A$. The harmonic cancellation has further deteriorated, and by similarly expanding the analysis, as in Section IV, the cross-over point can be calculated at $N = 2$. This result demonstrates that if the capacitors experience significant deviation from their target value then the harmonic performance of the PSC-PWM technique will quickly deteriorate. Similar to the previous analysis, there is a linear relationship between the distortion introduced by each carrier harmonic and the parameter which is causing the distortion, in this case the transient voltages present on the capacitors.

Remark 1: A cross-over point of $N = 2$ is well within the number of H-bridges used in a practical H-StatCom system. Therefore, the previously indicated clear superiority of the PSC-PWM scheme over SVM is no longer a clear cut issue when non-uniform DC bus voltages, carrier phase shift errors, and transient capacitor voltages are included in the modeling. ■

One important point to note here is that the harmonic deterioration will be a function of H-StatCom RMS voltage. The crucial parameter is the relative increase in voltage ripple with respect to the modulation index of each bridge i.e. if the voltage ripple difference between bridges is large and the effective pulse width is small then the resultant harmonic performance will be significantly poorer than if the voltage ripple remains the same but the pulse width (modulation index) is large. This is because under the second condition the modulation indexes and phase angles will differ significantly less between bridges in percentage terms.

Another important point is that the switching frequency of the SVM scheme can be reduced by exploiting the available redundancy in a H-StatCom. This can be achieved by Model Predictive Control (MPC) [9], [10]. MPC is similar to deadbeat

control in that a system model is used to determine the required control action. Where MPC differs is that the control action is chosen based on an optimality criterion. This means that models of the different system components can all determine the optimum control action. MPC also allows the models to be extended to include an arbitrary number of control cycles. This is referred to as increasing the prediction horizon. The predictions for the system variables are evaluated in a cost function which totals the errors associated with each model. The control action which minimises the total error is applied in the next control interval and the process is then repeated for each subsequent interval.

It is shown in [9] that by modifying the logic based algorithm which chooses which capacitors are used to create a voltage vector, it is possible to reduce the switching frequency at the expense of greater capacitor voltage ripple. This paper has stated that the harmonic performance of SVM is independent of the capacitor voltage ripple therefore any decreases in switching frequency brought about through the use of MPC will linearly decrease the cross-over point. [9] showed that the switching transitions can be reduced by a factor of three over the SVM scheme described in [6]. As an extension to this work the prediction horizon can be increased to further reduce the switching transitions. This means that in any one control interval the next two or three control intervals are investigated in terms of the system models evaluated in the cost function. This allows a penalisation of the next control interval's switching transitions based on where the current vector is heading further into the future. This will result in a reduction of switching losses and hence a reduction of the cross-over point where the performance of SVM becomes comparable to PSC-PWM.

V. Conclusions & Contributions

In Part 1 of this paper it was shown that due to variance in capacitor voltage ripple, phase-shift error and transient capacitor voltages the harmonic cancellation inherent to the PSC-PWM technique will deteriorate. This paper investigated a particular H-StatCom application and operational condition to determine the practical performance of the phase shifted modulation technique. The results indicate the harmonic performance is not greatly affected when only the non-uniform DC bus voltages are modeled, however when the example is expanded to consider phase-shift error and transient capacitor voltages the harmonic performance is significantly degraded. This degradation has been investigated to define the conditions under which the space vector modulation technique can have comparable performance to the phase-shifted technique, in a H-StatCom application.

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